AMENDMENTS TO THE SPECIFICATION

Please amend paragraph [0004] as follows:

[0004] The ability to access data having different data widths may result in unaligned data. As illustrated in FIG. 1, memory system 120 contains data sets A, B, C, D, E, and F. Each data set is separated as one or more half words (i.e., 16 bits wide) in memory system 120. For example, data set A includes half words ~~A1~~A0, A1, A2, and A3. Data set B includes half word B0. Data set C includes half words C0 and C1. Data set D includes half words D0, D1, D2, and D3. Data set E includes half word E0 and E1. Data set F includes half words F1, F2, F3, and F4 (not shown). Data set A, which is located completely in row 0, is aligned data and can easily be retrieved in one memory access. However, data set D is located in both row 1 and row 2. To retrieve data set D, CPU 110 must access memory system 120 twice. First to retrieve half word D0 in row 1 and then to retrieve half words D1, D2, and D3 in row 2.

Please amend paragraph [0019] as follows:

[0019] As explained above, conventional microprocessor systems do not provide adequate memory bandwidth for data sets stored in more than one row of a memory system. While using a dual port memory provides higher bandwidth, the cost in silicon area and power for the dual port memory prevents wide spread use of dual port memories. Furthermore, dual ported memory operate at lower frequencies than single ported memories. Co-pending U.S. patent application Ser. No. ~~_____ (Attorney Docket No. INF-025)~~10/777,570, entitled "FAST UNALIGNED MEMORY ACCESS SYSTEM AND METHOD", by Oberlaender, et al., herein incorporated by reference, describes a multi towered memory system that allows retrieval or storage of a data set on multiple rows of a memory system using a single memory access without the detriments

associated with a dual port memory system. The present invention describes a novel cache structure that supports unaligned accesses for multi-towered memory systems.